APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/608,637	06/30/2000	Jin Yang	42390.P9429	9275

7590	03/09/2004

Michael J Mallie
Blakely Sokoloff Taylor & Zafman LLP
12400 Wilshire Boulevard
7th Floor
Los Angeles, CA 90025

EXAMINER
GARCIA OTERO, EDUARDO

ART UNIT	PAPER NUMBER
2123	6

DATE MAILED: 03/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>*30 June 2000 and 12 May 2003*</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

    1.☐ Certified copies of the priority documents have been received.

    2.☐ Certified copies of the priority documents have been received in Application No. _____.

    3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
    application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date <u>*4, 5*</u>.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____ .

DETAILED ACTION: Non-Final (first action on the merits)

Introduction

1. Title is: METHODS FOR FORMAL VERIFICATION ON A SYMBOLIC LATTICE DOMAIN

2. First named inventor is: YANG

3. Claims 1-30 have been submitted, examined, and rejected.

4. The present US Application was filed 6/30/00, no earlier priority is claimed.

Index of Prior Art

5. **Jain** refers to "Formal Hardware Verification by Symbolic Trajectory Evaluation" by Alok Jain, Dissertation, July 1997.

6. **Chou** refers to "The Mathematical Foundation of Symbolic Trajectory Evaluation" by Ching-Tsun Chou, 1999.

Specification-objections-informalities

7. The Specification is objected to because of the following informalities. Appropriate correction is required.

8. At page 5, FIG 8a is described twice, and FIG 8b and 8c are not described at all.

35 USC § 112-Second Paragraph-indefinite claims

9. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. **Claims 1 and 5-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite** for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. Claim 1 states "initialize a symbolic simulation relation", and dependent claim 5 states "compute the symbolic simulation relation". It is not clear how the term "initialize" in independent claim 1 is distinct from (or broader than) the term "compute" in dependent claim 5.

12. Claim 6 is rejected for the same reasons as claim 5.

Claim Rejections - 35 USC § 102(b)

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action: A person shall be entitled to

a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country

or in public use or on sale in this country, more than one year prior to the date of application for patent in the

United States.

14. **Claim 1-30 rejected under 35 U.S.C. 102(b) as being anticipated by Jain.**

15. Claim 1 is an independent "recordable media having executable instructions" claim, and

claims 2-8 depend from claim 1 directly or indirectly.

16. In claim 1, **"initialize a symbolic simulation relation for an assertion graph on a first

symbolic lattice domain"** is disclosed by Jain page iii "The specification is defined as a set

of abstract assertions defining the effect of each operation on the user-visible state. An

implementation mapping is used to relate abstract states to detailed circuit states." And also

disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory

Evaluation (STE) to perform the verification task... extended STE to handle some forms of

nondeterminism."

17. In claim 2, **"join a Boolean predicate for an outgoing edge from an initial vertex in the

assertion graph with a symbolic antecedent labeling of an edge in the assertion graph"**

is disclosed by Jain page iii "The specification is defined as a set of abstract assertions

defining the effect of each operation on the user-visible state." And also disclosed by Jain

page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to

perform the verification task... extended STE to handle some forms of nondeterminism."

18. In claim 3, **"the symbolic antecedent labeling comprises a symbolic indexing function to

encode a plurality of antecedent labels for a plurality of assertion graph instances,

having at least one assertion graph instance on a second lattice domain different from

the first symbolic lattice domain"** is disclosed by Jain page iii "The specification is defined

as a set of abstract assertions defining the effect of each operation on the user-visible state.

An implementation mapping is used to relate abstract states to detailed circuit states." And

also disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory

Evaluation (STE) to perform the verification task... extended STE to handle some forms of nondeterminism."

19. In claim 4, **"the assertion graph on the first symbolic lattice domain is configurable to express a justification property to verify by computing the symbolic simulation relation"** is disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state. An implementation mapping is used to relate abstract states to detailed circuit states." And also disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to perform the verification task... extended STE to handle some forms of nondeterminism."

20. In claim 5 limitation [1], **"compute the symbolic simulation relation for the assertion graph on the first symbolic lattice domain"** is disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state. An implementation mapping is used to relate abstract states to detailed circuit states." And also disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to perform the verification task... extended STE to handle some forms of nondeterminism."

21. In claim 5 limitation [2], **"check the symbolic simulation relation to verify a plurality of properties expressed by a plurality of assertion graph instances, having at least one assertion graph instance on a second lattice domain different from the first lattice domain"** is disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state. An implementation mapping is used to relate abstract states to detailed circuit states." And also disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to perform the verification task... extended STE to handle some forms of nondeterminism."

22. In claim 6 limitation [1], **"compute the symbolic simulation relation for the assertion graph on the first symbolic lattice domain"** is disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state. An implementation mapping is used to relate abstract states to detailed circuit states." And also disclosed by Jain page 3 "Our methodology uses a technique called

Symbolic Trajectory Evaluation (STE) to perform the verification task… extended STE to handle some forms of nondeterminism."

23. In claim 6 limitation [2], **"compute the symbolic simulation relation for the assertion graph on the first symbolic lattice domain"** is disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state. An implementation mapping is used to relate abstract states to detailed circuit states." And also disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to perform the verification task… extended STE to handle some forms of nondeterminism."

24. In claim 7, **"join the symbolic simulation relation for the assertion graph on the first symbolic lattice domain, to any states that are contained by a symbolic antecedent for a first plurality of edges of the assertion graph on the fist symbolic lattice domain and also contained by a symbolic post-image for a second plurality of edged incoming to the first plurality of edges"** is disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state. An implementation mapping is used to relate abstract states to detailed circuit states." And also disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to perform the verification task… extended STE to handle some forms of nondeterminism."

25. In claim 8, **"compute the symbolic simulation relation for the assertion graph on the first symbolic lattice domain to verify the assertion graph according to a normal satisfiability criteria"** is disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state. An implementation mapping is used to relate abstract states to detailed circuit states." And also disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to perform the verification task… extended STE to handle some forms of nondeterminism."

26. Claims 9-30 are also all rejected, all limitations are disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state. An implementation mapping is used to relate abstract states to detailed

circuit states." And also disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to perform the verification task... extended STE to handle some forms of nondeterminism."

Additional Cited Prior Art

27. The following US patents or publications are hereby cited as prior art, but have not been used for rejection. Applicant should review these carefully before responding to this office action.

28. US Patent 6,539,345 discloses symbolic simulation using input space decomposition and "symbolic trajectory evaluation" at column 4 line 12.
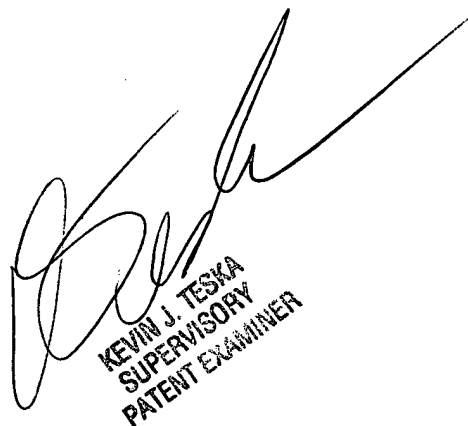
Conclusion

29. All claims stand rejected against prior art.

30. The specification is objected to, regarding the discussion of the figures.

Communication

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 703-305-0857. The examiner can normally be reached on Tuesday through Friday from 9:00 AM to 8:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone number for this group is 703-872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.   * * *